856 can also be stored in video memory 850. Alternatively, the frames can be stored in memory 830 or in some other memory. If, for example, motion compensation circuitry 840 were rendering a B frame a single frame would be read from video memory 850 for reconstruction purposes. In the example of Figure 8, four frames are stored in video memory 850; however, any number of frames can be stored in video memory 850.

A2 cont

IN THE CLAIMS

2. (Amended) The method of claim 1 wherein the first order is based on output from an Inverse Discrete Cosine Transformation (IDCT) operation.

3. (Amended) The method of claim 1 wherein performing frame prediction operations further comprises:

generating a bounding box containing the macroblock;

iterating the bounding box;

fetching reference pixels;

filtering the reference pixels;

averaging the filtered reference pixels, if necessary; and

adding correction data to the reference pixels.

A3 cont

7. (Amended) The apparatus of claim 6 wherein the first order is based on output from an Inverse Discrete Cosine Transform (IDCT) operation.

A4 Cont

8. (Amended) The apparatus of claim 6 wherein performing frame prediction operations further comprises:

means for generating a bounding box containing the macroblock;

means for iterating the bounding box;

means for fetching reference pixels;

means for filtering the reference pixels;

means for averaging the filtered reference pixels, if necessary; and

means for adding correction data to the reference pixels.

11. (Amended) A circuit for generating motion compensated video, the circuit comprising:

a command stream controller coupled to receive an instruction to manipulate motion compensated video data;

a write address generator coupled to the command stream controller;

a memory coupled to the command stream controller and to the write address generator, the memory to store pixel data in a first order determined by the write address generator;

processing circuitry coupled to the write address generator to receive control information and data from the command stream controller to generate a reconstructed video frame; and

a read address generator coupled to the processing circuitry and to the memory, the read address generator to cause the memory to output pixel data in a ~~second order.~~